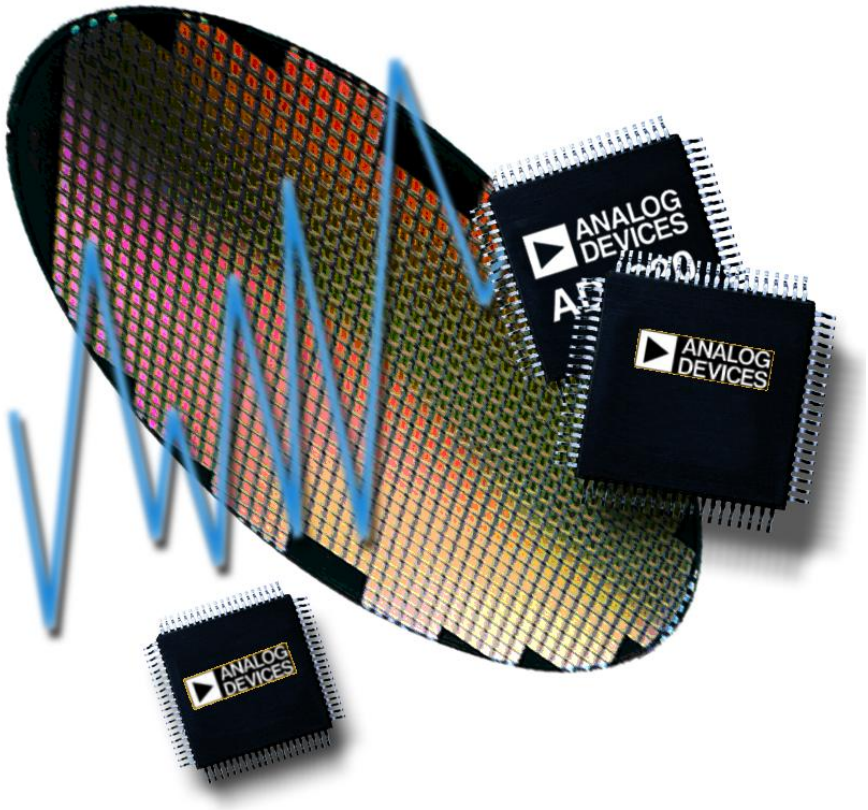

Reliability Report

Report Title: ADV7123/5 TSMC Fab9

Report Number: 7755

Revision: A

Date: 20 November 2009

Summary

This report documents the successful completion of the reliability qualification requirements for release of the ADV7123, ADV7125 products in both 48-LFCSP and 48-LQFP packages. The ADV7123 and ADV7125 are Triple high speed, D/A convertors on a single monolithic chip. They consists of three high speed, 10-bit and 8-bit video DACs with complementary outputs, a standard TTL input interface, and a high impedance, analog output current source respectively.

Table 1: ADV7123 Product Characteristics

Die/Fab

Maximum Power Dissipation (W)	0.450
Device / Die ID	V291A
Die Size (mm)	2.20 x 2.78
Wafer Fabrication Site	E_TSMC0908
Wafer Fabrication Process	0.60µm SPDM CMOS
Transistor Count	14 thousand
Passivation Layer	undoped-oxide/SiN
Bond Pad Metal Composition	AlCu
Die Overcoat	NA

Package/Assembly

Available Package	48-LFCSP
Body Size (mm)	7.00 x 7.00 x 0.85
Assembly Location	Amkor-K
Molding Compound	Sumitomo G700
Wire Type	Gold
Wire Diameter (mils)	1.00
Die Overcoat	NA
Die Attach	Ablestik 8290
Lead Frame Material	Copper
Lead Finish	Tin Plate
Moisture Sensitivity Level	3
Maximum Peak Reflow Temperature (°C)	260

Table 2: ADV7125 Product Characteristics

Die/Fab

Maximum Power Dissipation (W)	0.250
Device / Die ID	V291A
Die Size (mm)	2.20 x 2.80
Wafer Fabrication Site	E_TSMC0908
Wafer Fabrication Process	0.60µm SPDM CMOS
Transistor Count	14 thousand
Passivation Layer	undoped-oxide/SiN

Bond Pad Metal Composition	AlCu
Die Overcoat	NA

Package/Assembly

Available Package	48-LFCSP
Body Size (mm)	7.00 x 7.00 x 0.85
Assembly Location	Amkor-K
Molding Compound	Sumitomo G700
Wire Type	Gold
Wire Diameter (mils)	1.00
Die Overcoat	NA
Die Attach	Ablestik 8290
Lead Frame Material	Copper
Lead Finish	Tin Plate
Moisture Sensitivity Level	3
Maximum Peak Reflow Temperature (°C)	260

Description / Results of Tests Performed

Tables 3 and 4 provide a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Tables 1 and 2. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Table 3: Package Qualification Test Results

Test Name	Specification	Conditions	Device	Package	Lot #	Sample Size	Qty. Failures
Autoclave (AC)[1]	JESD22-A102	121°C 100%RH 2atm 96 hours	ADV7125	Amkor-K 48-LFCSP	Q7755.100	77	0
					Q7755.101	77	0
					Q7755.102	77	0
			AD1833A	STATS-C 48-LQFP	Q7494.1	77	0
					Q7494.4	77	0
					Q7494.7	77	0
			AD1938	STATS-C 48-LQFP	Q7506.1	77	0
					Q7506.2	77	0
					Q7506.3	77	0
			AD1940	STATS-C 48-LQFP	Q7529.1	77	0
					Q7529.2	77	0
					Q7529.3	77	0
EEPROM Endurance Cycling	JESD22-A117	25°C, 10K Cycles Single Duration	ADUC7032	STATS-C 48-LQFP	Q7217.24	77	0
Biased HAST (HAST)[1]	JESD22-A110	130°C 85%RH 2atm, Biased 96 hours	ADV7125	Amkor-K 48-LFCSP	Q7755.200	77	0
					Q7755.201	77	0
					Q7755.202	77	0
		130°C 85%RH 2atm, Biased 96 hours	AD1938	STATS-C 48-LQFP	Q7506.4	77	0
					Q7506.5	77	0
					Q7506.6	77	0
			AD1940	STATS-C 48-LQFP	Q7529.5	77	0
					Q7529.6	77	0
					Q7529.7	77	0
			ADUC7032	STATS-C 48-LQFP	f161421.21	77	0
					f161423.7	77	0
High Temperature Storage Life (HTSL)	JESD22-A103	150°C 1,000 hours	ADV7125	Amkor-K 48-LFCSP	Q7755.300	77	0
Solder Heat Resistance (SHR)[1]	ADI-0049	See Below	AD1940	STATS-C 48-LQFP	Q7529.12	11	0
					Q7529.13	11	0
					Q7529.8	11	0
			ADV7125	Amkor-K 48-LFCSP	Q7755.400	11	0
					Q7755.401	11	0
					Q7755.402	11	0
			AD1833A	STATS-C 48-LQFP	Q7494.2	11	0
					Q7494.5	11	0
					Q7494.9	11	0
			AD1938	STATS-C 48-LQFP	Q7506.7	11	0
					Q7506.8	11	0
					Q7506.9	11	0
			ADUC7032	STATS-C 48-LQFP	Q7217.21	77	0
					Q7217.23	77	0
Temperature Cycling (TC)[1]	JESD22-A104	-65°C / +150°C 500 cycles	ADV7125	Amkor-K 48-LFCSP	Q7755.500	77	0
					Q7755.501	77	0
					Q7755.502	77	0

			AD1833A	STATS-C 48-LQFP	Q7494.10	77	0
					Q7494.3	77	0
					Q7494.6	77	0
			AD1938	STATS-C 48-LQFP	Q7506.10	77	0
					Q7506.11	77	0
					Q7506.12	77	0
			AD1940	STATS-C 48-LQFP	Q7529.10	77	0
					Q7529.11	77	0
					Q7529.9	77	0
			ADUC7032	STATS-C 48-LQFP	f161421.25	77	0
					f161422.4	77	0
					f161424.7	77	0

1) These Samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125ºC, Soak: Unbiased Soak: 192 hrs @ 30ºC, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260ºC.

Table 4: Process Qualification Test Results

Test Name	Specification	Conditions	Device	Fab Process	Lot #	Sample Size	Qty. Failures
Early Life Failure Rate (ELFR)	MIL-STD-883, Method 1015	125°C 48 hours	ADW84402	E_TSMC0908 0.6um CMOS,	Q6248.20	800	0
					Q6248.21	800	0
					Q6248.24	800	0
Biased HAST (HAST)[1]	JESD22-A110	130°C 85%RH 2atm, Biased 96 hours	AD8692	E_TSMC0908 0.6um CMOS	Q7248.8	77	0
					Q7248.9	77	0
					Q7248.10	77	0
			ADUM1402W	E_TSMC0908 0.6um CMOS,	Q7170.14	45	0
					Q7170.15	45	0
					Q7170.16	45	0
			ADW84402	E_TSMC0908 0.6um CMOS,	Q6248.13	45	0
					Q6248.14	45	0
					Q6248.22	45	0
High Temperature Operating Life (HTOL)[1]	JESD22-A108	125°C ‹ Tj ‹ 135°C, Biased 1,000 hours	ADUM1402W	E_TSMC0908 0.6um CMOS,	Q7170.12	45	0
					Q7170.13	45	0
					Q7170.11	45	0
		150°C ‹ Tj ‹ 175°C, Biased 1,000 hours	ADW84402	E_TSMC0908 0.6um CMOS,	Q6248.10	45	0
					Q6248.11	45	0
					Q6248.12	45	0
		150°C ‹ Tj ‹ 175°C, Biased 500 hours	AD8601	E_TSMC0908 0.6um CMOS	Q7507.3	77	0
			AD8692	E_TSMC0908 0.6um CMOS	Q7248.11	77	0
High Temperature Operating Life (HTOL)		125°C ‹ Tj ‹ 135°C, Biased 1,000 hours	ADV7123	E_TSMC0908 0.6um CMOS	OF67792.4	45	0
					OF67995.4	45	0
					OF67996.4	45	0

1) These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following: Bake: 24 hrs @ 125ºC, Soak: Unbiased Soak: 168 hrs @ 85ºC, 85%RH, Reflow: 3 passes through an oven with a peak temperature of 260ºC.

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site.

ESD Test Results

The results of ESD testing are summarized in the ESD Results Table. All parts were electrically tested at room and hot temperatures pre- and post-stress. ADI measures ESD results using stringent test procedures based on the specifications listed in Table 5. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook (available via the 'Quality and Reliability' link at http://www.analog.com).

Table 5: ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM Corner Pins Only	48-LFCSP	ANSI/ESD STM5.3.1-1999	1Ω, Cpkg	±750V	±1000V	C5
FICDM Corner Pins Only	48-LQFP	ANSI/ESD STM5.3.1-1999	1Ω, Cpkg	±750V	±1000V	C5
FICDM	48-LFCSP	ANSI/ESD STM5.3.1-1999	1Ω, Cpkg	±500V	±1000V	C4
FICDM	48-LQFP	ANSI/ESD STM5.3.1-1999	1Ω, Cpkg	±500V	±1000V	C4
HBM	48-LQFP	ANSI/ESD STM5.1-2007	1.5kΩ, 100pF	±1000V	±1500V	1C
MM	48-LQFP	ANSI/ESD STM5.2-1999	0Ω, 200pF	±150V	±200V	M2

Latch-Up Test Results

Six samples of the ADV7123 were Latch-up tested per JEDEC Standard JESD78, Class II, Level A. All six devices passed.

Approvals

Reliability Engineer: Colm Heffernan
This report has been approved by electronic means (4.0)

Additional Information

Data sheets and other additional information are available on Analog Devices' web site:
http://www.analog.com